Furthermore, functional units were separated to minimize electrical crosstalk:
With one exception, only the 8 current regulator circuits are placed on the bottom layer of the PCB. For detection of the optical signal, the OPT101 photodiode is also placed on the bottom layer and surrounded by regions on GND potential to shield from current regulator influences.
Electromagnetically isolated by the mid GND and VCC planes, the rest of the components is placed on the top layer. Thus, especially post-amplification, lock-in demodulation and filtering processes are shielded against electrical noise from current modulation processes. Sensible signal lines on all layers were routed as far away from potential noise sources as possible.
The complete layout of the fNIRS module is depicted in figs. A.5 and A.6 in the appendix.

3.5 Hardware Design NIRS Mainboard

In this section, the detailed implementation of the system concept's NIRS mainboard elements will be described. To do so, the functional units are viewed individually and implemented under consideration of the findings in earlier sections and using the results of evaluation and testing of 3 prototype versions that were designed in the course of this work.
For the full schematics, please refer to figs. A.7 and A.8 in the appendix.

3.5.1 Power Supply

All elements and integrated circuits on the NIRS module and mainboard were selected for low-voltage symmetric operation. To supply the NIR light emitters, detector, amplifiers, conversion and communication units with power, a dual $\pm 5\,V$ power supply was designed for the mainboard.
For mobility and safety reasons, batteries are used as power source. This has another great advantage: Since no rectification and filtering is necessary to get a clean dc output, the overall complexity of the power supply design is reduced.

An estimation of the maximum peak currents resulted in a minimum current of $200\,mA$ (consisting mainly of $100\,mA$ for the LED emission unit and $60\,mA$ for the Bluetooth module), that needs to be supplied without significant drop of the supply voltage.
As the availability of negative voltage, low-dropout regulators ($-5\,V$ rail) in this power range is very limited, common fixed-voltage regulators are used. Regarding efficiency, these are in fact not the optimal choice for battery-powered applications but were the best compromise so far. Step-down regulators were not considered as an alternative to preclude possible noise/error influences resulting from the high-frequency chopping process.

The dual power supply design that was implemented for the NIRS instrument (see fig. 3.16) is based on MC7805 and MC7905 $1\,A$ positive and negative voltage regulators from ON Semiconductor and the design considerations in the MC7900 and MC7800 series datasheets.
To ensure good high-frequency characteristics ($3\,kHz$ LED modulation) and stable operation under all load conditions, $10\,\mu F$ bypass tantalum capacitors with low internal impedance at high frequencies are placed directly at the regulator inputs. Further $100\,nF$

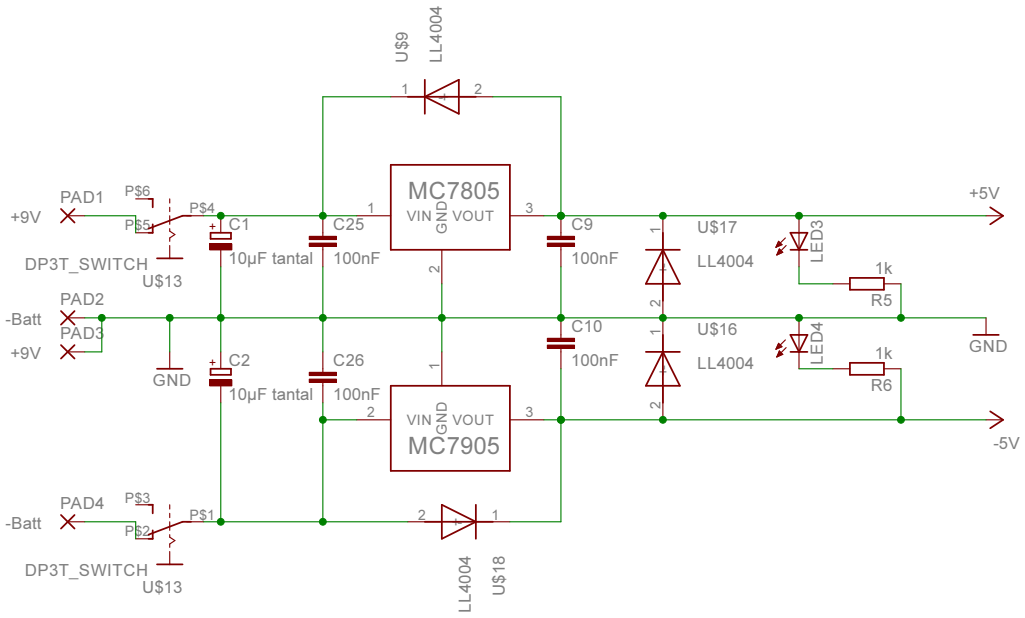

Figure 3.16: NIRS power supply.

bypass capacitors are placed at the in- and outputs.
For opposite polarity and reverse-bias protection, 1N4001-equivalent LL4004 diodes are used in the design.

For the input power supply rails, any battery (packages) with $> 7.4\,V$ can be used. In the first prototypes, $9\,V$ NiMh batteries were applied, enabling about 2 hours of continuous use. The final version of the instrument operates on two $6 \cdot 1.5\,V$ AA battery packages, allowing continuous usage for approximately 10 hours. A more expensive but possibly good alternative optimizing usability aspects (capacity, weight and recharging characteristics) would probably be the use of Li-Ion/Li-Polymer-battery packages from rc-car/hobby applications.

3.5.2 Analog-to-Digital Conversion

The NIRS mainboard provides four slots for NIRS modules. Thus, a total of 16 channels can be used. Even though the channels are time-division multiplexed and hence four NIRS channels of one module require only one analog-to-digital conversion (ADC) unit, four different physical lines have to be taken into account when all modules are to be used.
At the same time, high dc accuracy and quantization depth are necessary for a high-quality digital fNIRS signal representation.

For this reason, the LTC2486, a $16\,Bit$ 4-channel sigma-delta ADC from Linear Technology with integrated temperature sensor and $50/60\,Hz$ line-frequency rejection and very low noise ($600\,nV\,RMS$) was selected.
The LTC2486 provides a 4-wire SPI interface for configuration and data readout and an integrated 4-channel analog MUX. Using this integrated multiplexer, all four analog NIRS module lines can be digitized by one ADC.

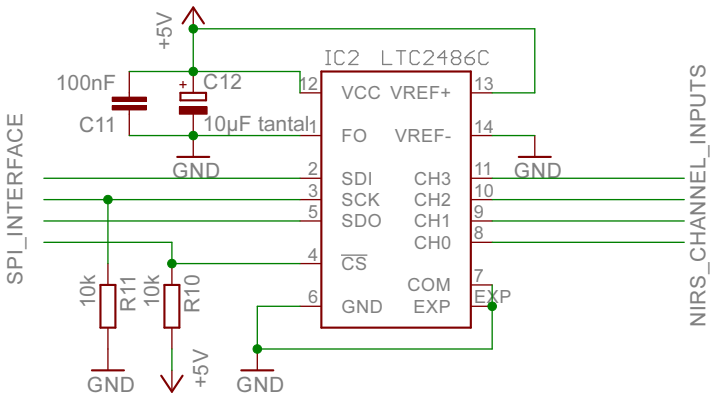

Figure 3.17: Analog-to-digital conversion (LTC2486).

To decouple the ADC from power supply variations, the VCC supply pin is stabilized by a $10\,\mu F$ tantalum bypass capacitor in parallel with a $100\,nF$ capacitor as recommended by the manufacturer.
Because of the high accuracy and internal noise rejection techniques and using an internal oscillator, the ADC allows a maximum sampling rate of $15\,Hz$. Even though the NIRS signal is a very slow dc signal (see section 2.2) and low sampling rates are therefore often sufficient, this would not be enough for simultaneous use of all 16 channels. With the SPI bus as communication interface, an increase of the overall sampling rate by scaling the number of ADCs on the mainboard design can easily be done. As this work focused on the NIRS module design, and the funds available for the instrument's design were limited and a few simultaneously active channels for BCI-trials are usually enough, this limitation was accepted for the time being.

Further design aspects regarding the ADC will be discussed in sections 3.5.5 (layout and shielding practice) and 3.7.2 (software implementation).

3.5.3 Communication/Bluetooth Transmission

For control and data transmission between the NIRS instrument and any host computer, the UART interface of the on-board microcontroller is used. This UART interface can be accessed by two means: By an ordinary RS232 wired connection or, as one aim of this work was to design the system for maximum mobility, via Bluetooth.
For the Bluetooth transmission, an embedded class 2 Bluetooth module by Amber Wireless was selected: The AMB2300 is a fully functional Bluetooth module with integrated LMX9830 antenna, configurable baud rate and several available integrated supported profiles. Using the Serial Port Profile in transparent mode, this module emulates a simple RS232 cable connection. Thus, with the software on the mainboard's microcontroller unit being implemented to support both modes of communication - wired and via Bluetooth - either one can be used.
In the latest prototype version of the mainboard, the interface is selected simply by using jumpers for the on-board Bluetooth module or a cable to a RS232 level converter unit with RS232 connector (see fig. 3.18).

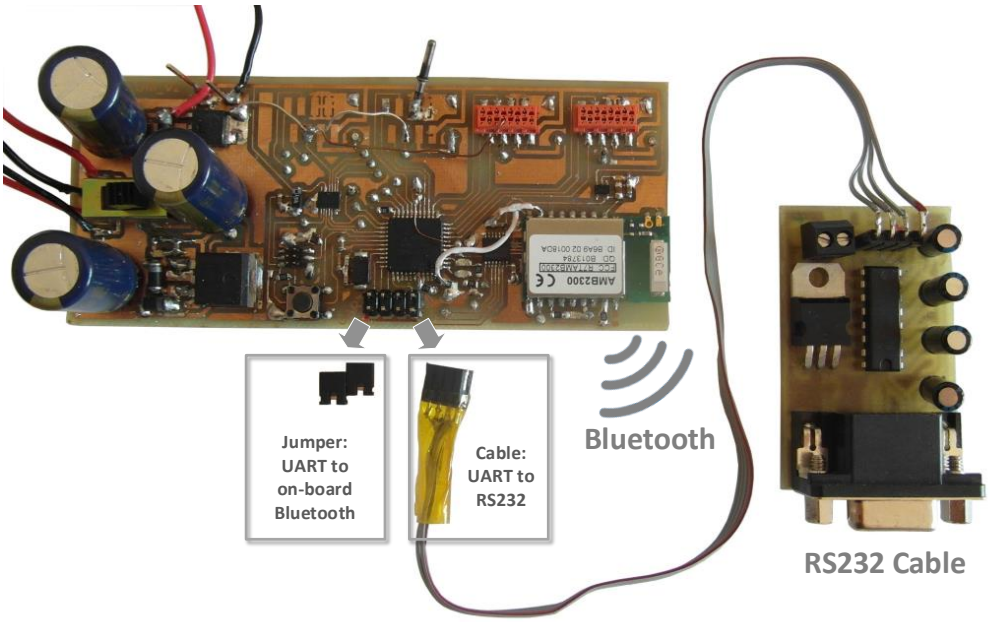

Figure 3.18: Communication interface: interface selection.

Implementing the support of a physical connection between the instrument and a PC without the use of the wireless module made the system suitable for a much better step-by-step hardware and software design testing and debugging.
Evaluation of the mainboard hardware and signal quality revealed that the Bluetooth module's high-frequency signals can generate significant electrical crosstalk to the on-board analog signal lines for analog-to-digital conversion. This crosstalk superimposes the amplified NIRS signal strongly enough for the signal to appear purely noisy after AD conversion. Fig. 3.19 shows the effect of the Bluetooth module signals on the analog dc NIRS signal (blue). $400mV$ peak-to-peak "Byte" noise distorts the signal significantly.

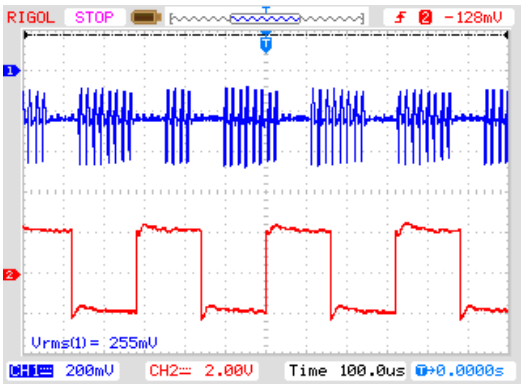

Figure 3.19: Bluetooth crosstalk on NIRS signal. Red: lock-in demodulator output, blue: low-pass output with Bluetooth interference.

To resolve this problem in the final version of the NIRS instrument (see fig. 3.20), the Bluetooth module and its peripheral hardware is placed on a separate PCB and is physically and electromagnetically separated by a metal shield surrounding the mainboard hardware. With the same interface selection concept as in fig. 3.18, the connector on the mainboard can either be used for the external Bluetooth PCB or for the RS232 level converter PCB.

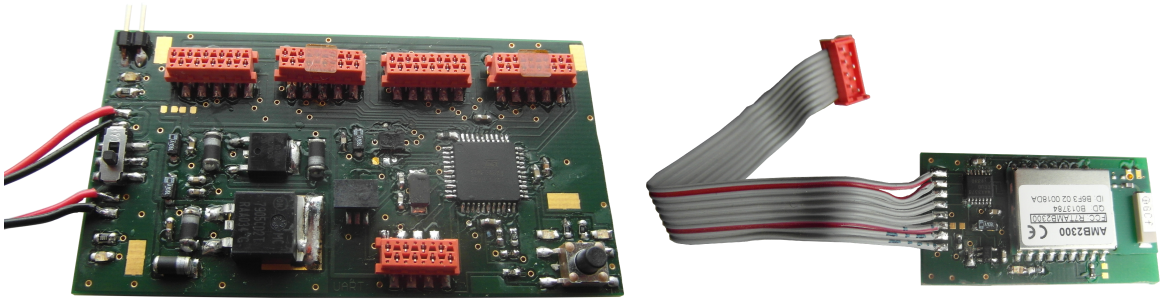

Figure 3.20: Final mainboard concept with separated Bluetooth module (right).

Figure 3.21 shows the hardware implementation of the final Bluetooth module PCB.

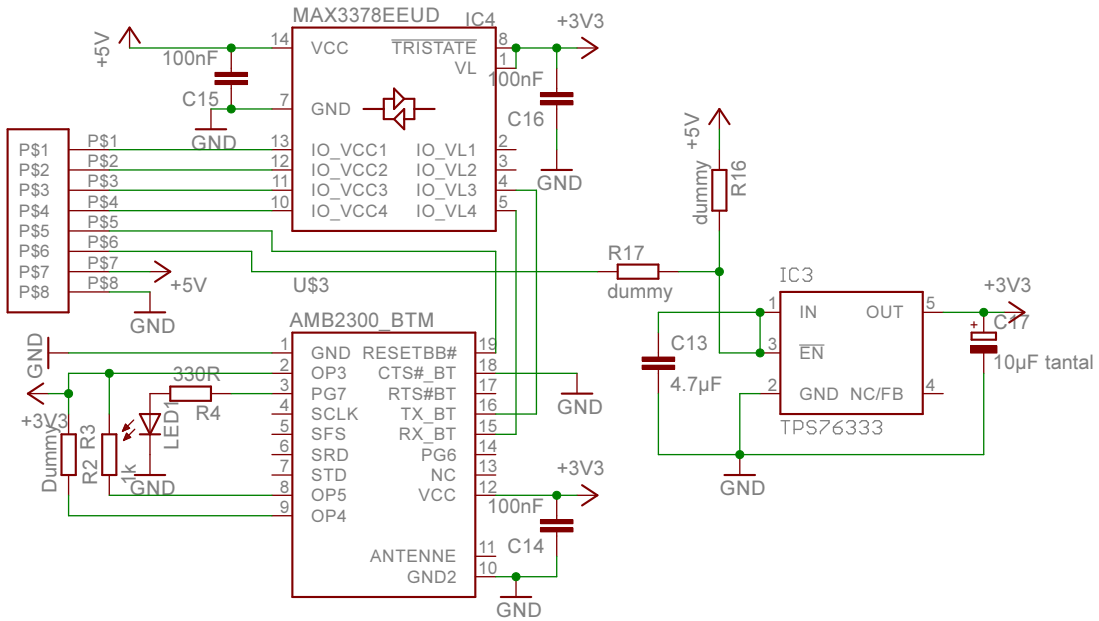

Figure 3.21: Hardware implementation of the Bluetooth module.

As the AMB2300 needs a $3.3V$ voltage supply, a TPS76333 low-dropout regulator (LDO) creates the $3.3V$ supply from the mainboard's $+5V$ rail. To minimize effects on the $+5V$ rail by the Bluetooth module supply currents, a $4.7\,\mu F$ input and a $10\,\mu F$ tantalum output bypass capacitor are placed closely by the in- and output pins of the LDO. The

input source ($+5\,V$ regulated or $+9\,V$ unregulated from the battery) can be selected by connecting one of two possible dummy $0\,R$ resistors.
As a result from the operation on different supply voltages, the digital voltage levels for the communication between microcontroller and AMB2300 have to be level shifted. A bidirectional level translation integrated circuit by maxim integrated (MAX3378) was selected for this purpose.
The AMB2300 Bluetooth module is externally hardwired for a baud rate of $9.6\,kbps$ and a LED is connected for status display.

3.5.4 Microcontroller Unit

For the control of the NIRS module channels and the analog-to-digital converter and for communication with a pc, an Atmel Corporation AtMega644 $8\,Bit$ microcontroller with $64\,kBytes$ in-system programmable flash and advanced RISC architecture was used.
The AtMega644 provides a programmable serial USART and a master/slave SPI serial interface, one $16\,Bit$ and two $8\,Bit$ timers/counters and 32 programmable I/O lines.

To guarantee the necessary accuracy for USART baud rate generation and to use the maximum possible processing speed, an external 20MHz crystal is applied. The design considerations are identical to the ones for the AtMega16A crystal in subsection 3.4.5.
For the generation of the USART baud rate and the selection of a proper crystal, some rules have to be followed to ensure error-free data transmission. The $8\,Bit$ baud rate register UBRR in the AtMega644 has to be configured using equation 3.18 (see AtMega644 datasheet)

$$UBRR = \frac{oscillatorfrequency(Hz)}{16 \cdot baudrate(bps)} - 0.5 \tag{3.18}$$

Since the value for UBRR has to be rounded, deviations of the generated frequency from the correct baud rate occur. For an error free data-transmission, the error

$$Error_{baud}[\%] = |(\frac{(UBRR_{rounded} + 1}{UBRR_{exact} + 1} - 1) \cdot 100| \tag{3.19}$$

has to be less than 1%.
For the chosen baud rate of 9600 and a 20MHz crystal $UBRR_{exact}$ is 129.208 and $UBRR_{rounded}$ is 129, resulting in an $Error_{baud} = 0.16\%$. Therefore, the crystal can be used.

For an automated start of the pre-configured instrument in an experiment, an external hardware trigger is implemented. It can be used, for example, to synchronize the start of a measurement with a certain condition becoming true, such as a button being pressed, a light sensor on a screen being illuminated, and so on. A jumper connector for those digital/analog control signals is provided on the mainboard. The input signal is analog-to-digital converted by one of the integrated $10\,Bit$ ADCs for comparison with a programmable threshold. When the control crosses the threshold line, a corresponding log-message is inserted into the UART data stream.

For status signals and debugging puproses, two LEDs are provided.

3.5.5 General Remarks on Layout and Design

As during the design of the NIRS module, the rules for good design practice were followed as well as possible and all supply pins of integrated circuits are buffered with $100nF$ capacitors.
For the final NIRS mainboard, a 4-layer PCB was designed (see fig. 3.22):

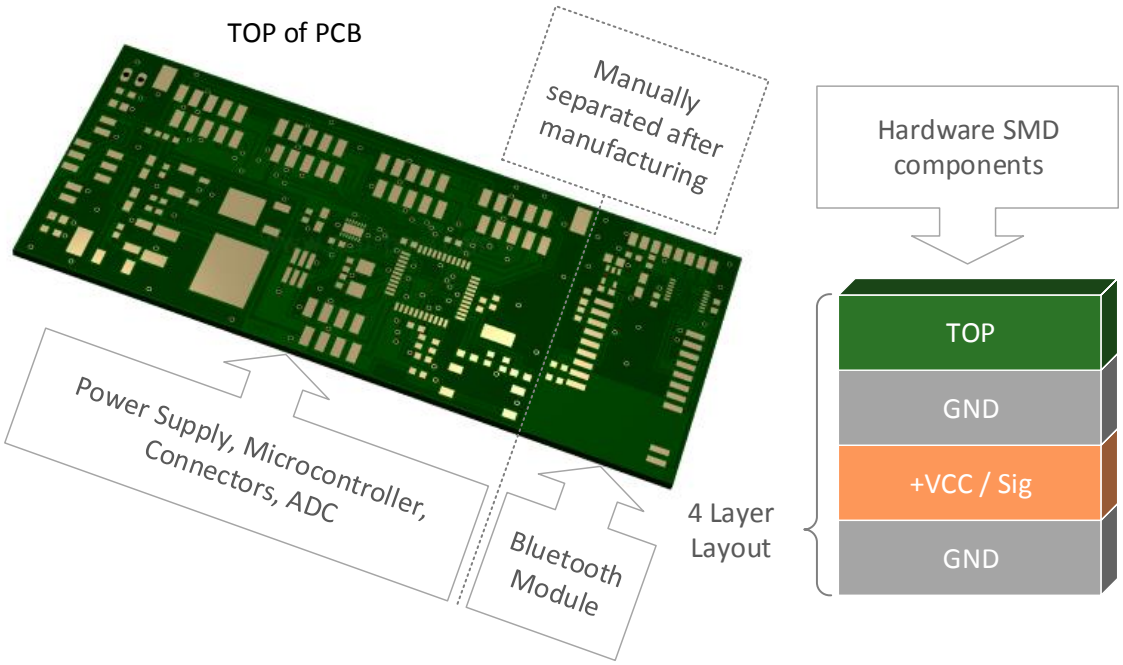

Figure 3.22: Layout of NIRS mainboard (using a PCB preview from www.pcb-pool.com).

The second and the fourth layer are designed as GND planes. Sensitive signal lines, such as the ones carrying the analog fNIRS signals from the connectors to the ADC, are routed between both GND planes and are thus shielded from external electric crosstalk coming from the Bluetooth module and other noise sources.
Below and around the ADC, only ground potentials, digital ADC control lines and analog signals are routed to further minimize noise pickup.

For cooling by passive heat distribution, the areas around and connected with the heat sinks of the voltage regulators are as large as possible.

On the Bluetooth module PCB, keep-out areas below and around the Bluetooth antenna were designed as specified by the manufacturer to minimize range attenuation by metallic elements.
To save manufacturing costs, the Bluetooth module and mainboard are designed in a single layout and manually separated after production.
The complete layout is depicted in fig. A.9 in the appendix.