4

Evaluation and Analysis

The NIRS instrument design process involved many evaluation and debugging steps that were often conducted iteratively. Results of these evaluation steps were integrated in successive versions of the instrument. Throughout the development phase, one evaluation board, 3 mainboard prototypes, 3 NIRS module prototypes and one respective final version were developed, each succeeding version gradually improving the instrument's design. The results of this process and the most important insights during design and evaluation of the functional elements are elaborated in the corresponding design sections in the previous chapter 3.
To characterize the whole system, however, particular characteristics were further evaluated and analyzed and will be discussed in the following section. After that, the results of physiological measurements and BCI trials for system verification and validation will be presented.

4.1 Evaluation of Hardware and Design

4.1.1 PWM Signal

The deviation of the 3.125 kHz PWM signal from an ideal square-wave reference for lock-in (de-)modulation was investigated. Fig. 4.1 shows the signal characteristics: The microcontroller's PWM module produces a stable square-wave signal with 27.2 ns rise and 19.6 ns fall times. Fourier power spectrum analysis reveals clean 3.125 kHz peaks and higher harmonics.

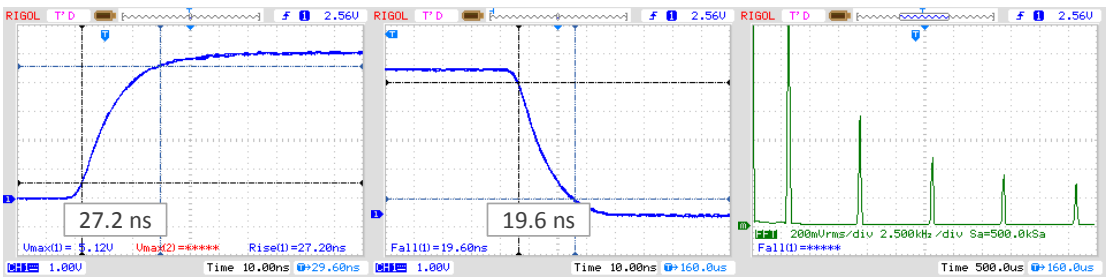

Figure 4.1: PWM signal characteristics at the microcontroller output.

As mentioned in subsection 3.4.3, the PWM signal is level shifted by a voltage divider for zero crossing detection in the lock-in demodulator. The RC network that results from the high-ohmic voltage divider resistors and PCB line capacities affects the PWM signal propagation: It creates an effective propagation delay of the signal's zero crossing of approximately $4\,\mu s$.
Even though this delay was not intended, it has a positive effect on the demodulation during lock-in detection: It compensates for $4\,\mu s$ of the phase shift between the microcontroller PWM reference for current modulation and the incoming pre-amplified photodetector signal that is to be demodulated. Thus, the attenuation resulting from demodulation (see subsection 4.1.4) is reduced.

4.1.2 Power Supply

For the power supply, two different characteristics were evaluated: DC supply voltage drifts during signal acquisition, and current modulation impacts on the supply voltage.

The DC supply voltage drift measurements yielded a stable supply voltage of $+4.959\,V$ and $-4.960\,V$ with $< 500\,\mu V$ drift in 20-minutes measurement periods. However, when the device was started after being inactive for several hours, a supply voltage stabilization period of several seconds was observed. Possibly due to battery voltage recovery during off-times, a voltage regulator output drop of up to $20\,mV$ in a period of $< 20\,s$ takes place until the output voltage reaches a stable level. Thus, prior to signal acquisition, a waiting cycle of $20\,s$ after initial instrument power-up is recommended.

To investigate the impacts of the $3.125\,kHz$ current modulation on the power supply and thereby on the photodetector and signal amplification components, their output signals were evaluated during active modulation but without optical input to the sensor. For this purpose, the active NIR LED was placed in an opaque metal box and the photodetector was covered with opaque sticky tape.
To evaluate the maximum impact of the current modulation on the signal, the LED was modulated using the maximum DAC current level ($100\,mA$, DAC level 4). To specify whether the current modulation effects can be minimized by using different voltage supplies, the measurements were done with two different sources for the LED current (for reference, see VCC in fig. 3.12): First, the mainboard's $+5\,V$ regulated voltage rail common for all hardware elements was used, then the LED current was supplied directly from the $+9\,V$ battery voltage. Figure 4.2 shows the resulting ouptut signals of the OPT101 photodetector and the PGA during current modulation without optical input to the sensor.
The current modulation flanks create a $\pm 2\,mV$ high-frequency noise around the sensor output baseline signal that is further amplified by the PGA to strong $\pm 100\,mV$ peaks. Supplying the current directly from the battery to minimize impacts on the regulated $+5\,V$ does not improve this.
However, an influence on the baseline of the signal could not be observed and high-frequency noise is effectively suppressed by the 3rd-order lock-in low-pass. Therefore, these effects are presently considered not crucial. Yet, in future power supply design approaches, high-frequency decoupling of the supply voltage is recommended.

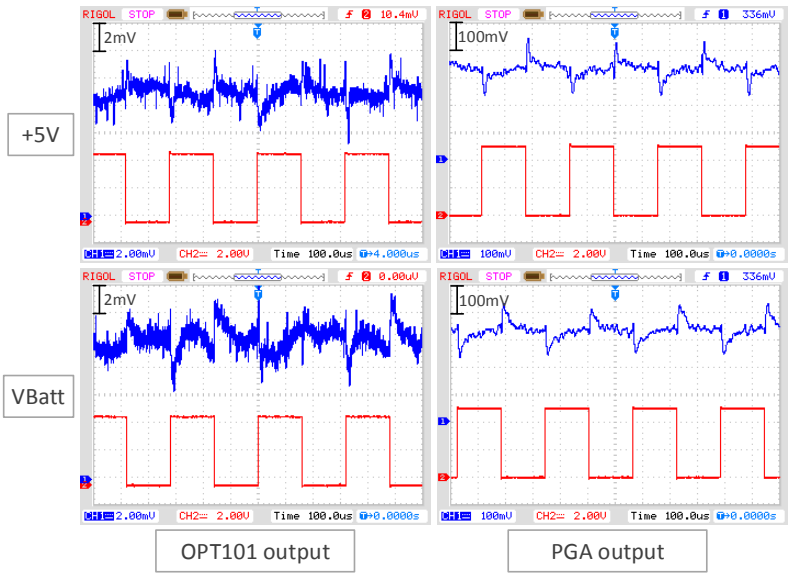

Figure 4.2: Current modulation impacts on signal detection and amplification path. Blue: output signals, red: PWM modulation reference.

4.1.3 Current Regulators

To optimize the current regulator performance, the selection of the operational amplifier was based on an evaluation of speed and oscillation characteristics of two high-precision types (LMC6064 and AD824A) that were considered for the design. As indicated by the slew rates specified by the manufacturer (LMC6064: $35\,V/ms$, AD824A: $2\,V/\mu s$), the AD824A enables a much faster current regulation than the LMC6064 (see fig. 4.3).

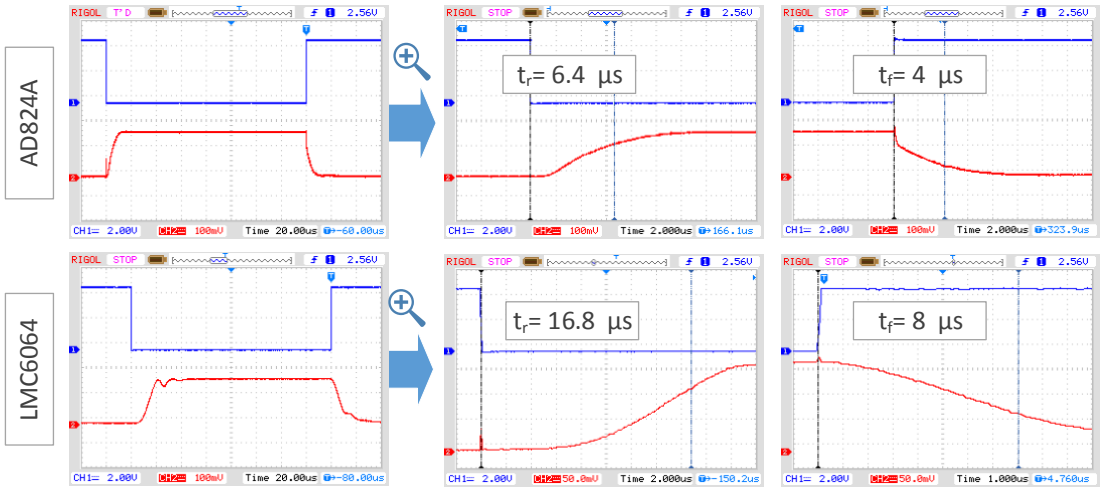

Figure 4.3: Evaluation of LMC6064 and AD824A speed. Blue: PWM reference, red: modulated LED current signal. Measured over 1Ω resistance with inverted analog switching logic using DAC level 4.

With a rise time of $t_r = 6.4\,\mu s$ and a fall time of $t_f = 4\,\mu s$, the AD824A provides more than twice the edge steepness of the square-wave current signal compared to the LMC6064 ($t_r = 16.8\,\mu s$, $t_f = 8\,\mu s$). Also, in the LMC6064, higher transient oscillation and settling were observed than in the AD824A. Thus, despite higher costs, the AD824A was selected for the current regulator design.

To minimize transient oscillation and settling times, a decoupling capacitor was introduced between operational amplifier negative input and output (see also subsection 3.4.4). To determine the optimal value of this capacitor, both LTSpice simulations and experiments were conducted. Fig. 4.4 shows an excerpt of a series of measurements that has been conducted for this purpose. For two current levels (DAC lvl 2 = $80\,mA$ and DAC lvl 4 = $100\,mA$) the shape of the regulated current signal was investigated with C= 0, $4.7\,pF$, $10\,pF$, $33\,pF$, $100\,pF$, $200\,pF$ and $330\,pF$ (see fig. A.14 for a comparison of all measurements).

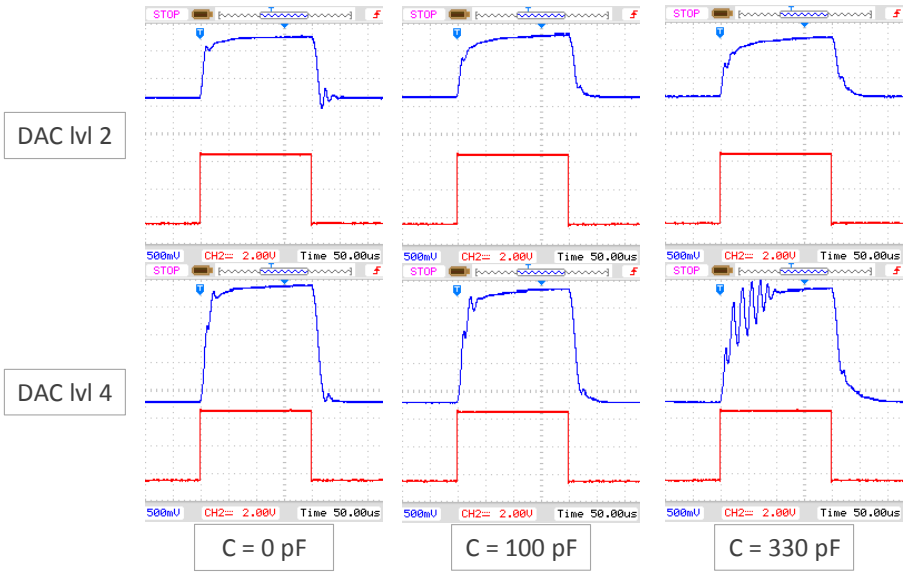

Figure 4.4: Evaluation of optimal current regulator decoupling capacitor value (excerpt). Blue: voltage (implying LED current) measured at LED cathode, red: PWM modulation reference.

The experimental results indicated that for lower current levels the use of low decoupling capacities intensifies oscillations during the settling of the signal. For higher current levels, higher decoupling capacities increase the transient oscillation of the signal. To optimize the signal for minimal oscillations and maximal edge steepness for all DAC levels, the decoupling capacitor value was chosen to be $100\,pF$.

Figure 4.5 shows the shape of a DAC lvl 4 regulated and $3.125\,kHz$ modulated square-wave current signal resulting from the final current regulator design.

4.1.4 Lock-In Detection

Using the mathematical description of lock-in modulation/demodulation from section 3.4.3, the effects of phase shifts between the PWM reference and the signal at the lock-in

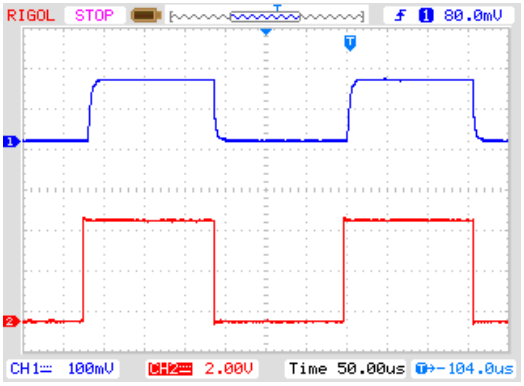

Figure 4.5: Shape of modulated current signal at DAC level 4. Blue: Current measured over 1Ω resistor, red: PWM reference.

demodulator input due to propagation delays were evaluated.

From equation 3.16 it is obvious that the signal's attenuation resulting from a phase shift is proportional to the cosine of this phase shift: $\cos(\Phi_S - \Phi_R)$. With

$$\Phi_S - \Phi_R = \frac{\Delta t}{T} \cdot 2\pi, \tag{4.1}$$

Δt being the total propagation delay of the signal and T being the cycle duration, the resulting attenuation A of the signal caused from lock-in demodulation can be estimated using

$$A = \cos\left(\frac{\Delta t}{T} \cdot 2\pi\right). \tag{4.2}$$

To minimize effects due to propagation delays, all hardware elements in the signal path were selected with respect to high-speed/low delay times. Figure 4.6 shows a measurement of the total resulting phase shift between the PWM reference and the demodulator input in the final hardware design.
For an approximation of the total effective phase shift, delays between the signals were measured at the 50% levels of both rising and falling edges respectively. The total phase shift effecting the attenuation by demodulation is the sum of times where signal and reference levels do not overlap, thus $\Delta t = t_{dr} + t_{df} = 18.5 + 7.2\,\mu\,s$. This phase shift results mainly from the total propagation delays from demultiplexer, analog switches, current regulator, photodetector and PGA. Using eq. 4.2, the attenuation factor A caused by non-phase-synchronous demodulation of the signal with a cycle duration of $T = 320\,\mu s$ is estimated as approximately 0.875.

Fig. 4.7 depicts the effect of the phase shift on the demodulated signal.
The pre-amplified signal from the photodetector (red) is multiplied with the sign of the square-wave reference (not in the picture). In the demodulated signal (blue), the phase shift results in an inversion of parts of the input signal carrying functional information to below-zero levels and parts of the noise and stray light signal to a positive level respectively.

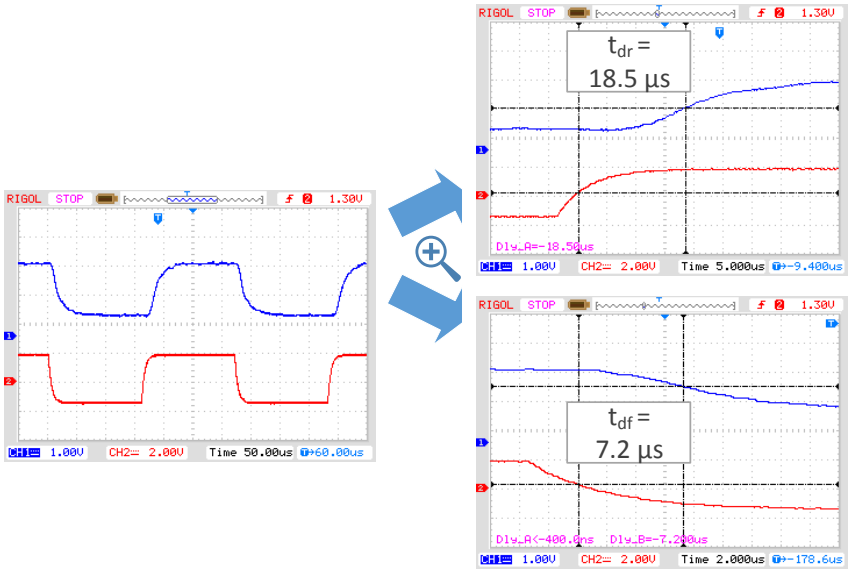

Figure 4.6: Measurement of total phase shift between PWM reference input and demodulator input. Blue: signal at demodulator input, red: PWM reference input.

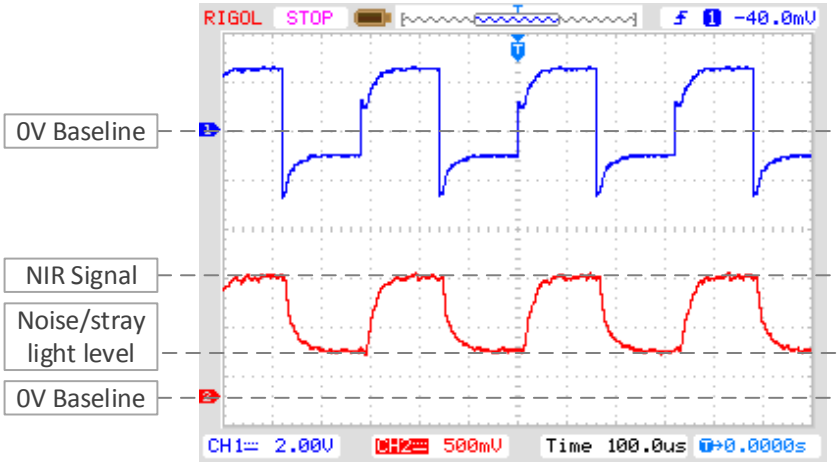

Figure 4.7: Attenuation effect of phase shift on demodulation. Blue: demodulated signal, red: lock-in input signal.

To further minimize the attenuation resulting from phase shift, four approaches are possible:

1. Using digital lock-in amplification,
2. Using two-phase quadrature amplification,
3. Using even faster hardware components in the signal path,
4. Adding an arbitrary shift in the reference signal path using elements for small delays.

The 3rd and 4th approaches offer a promising perspective, as only minor concept design adaption is necessary. Especially the programmable gain amplifier's (PGA) contribution

to the phase delay can be reduced significantly: It was measured as 7 μs and 4.5 μs for rising and falling edges respectively.

4.1.5 System Drift

Several factors were considered to be possible sources of system drift:

- Changes in the 1 Ω current regulation resistance due to temperature changes resulting in variations of the LED current.
- Changes in the total radiated power of the LEDs despite constant currents due to temperature changes in the semiconductor junction.
- Supply voltage variations.

Changes in stray light, amplifier and thermal resistor noise are strongly suppressed by the lock-in amplification process.
To minimize signal drifts resulting from changes in the 1 Ω current regulator resistance, Panasonic current sensing resistors with a low temperature coefficient of resistance ($TCR = \pm 50 \cdot 10^{-6}/°C$) were chosen.
To evaluate the effective overall system drift, the fNIRS module was placed in an opaque closed box to screen it from background radiation. With a fixed module position and thus fixed NIR light reflection intensity in the box, the signal of one DAC level 4 active channel in speed mode was constantly acquired for 10 minutes (see fig. 4.8).

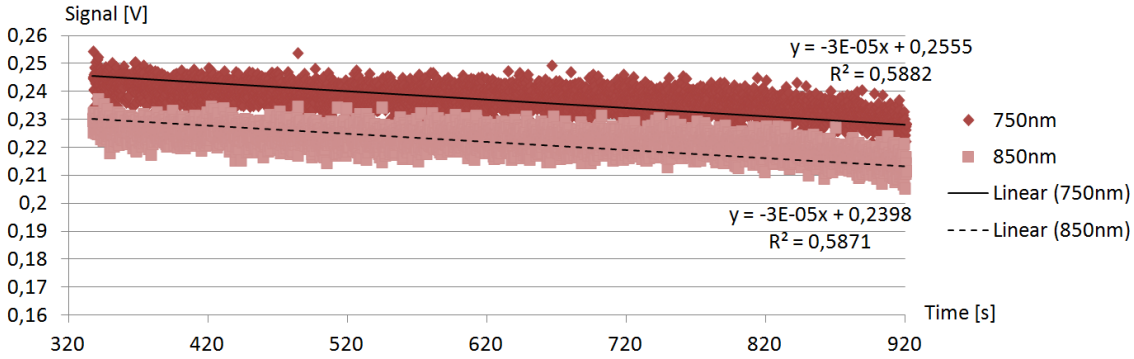

Figure 4.8: Overall system drift characterized by linear least squares approximation.

The drifts of both wavelength signals were approximated using a linear least squares regression method. The regression yielded a negative drift coefficient of $C_D = -3{\cdot}10^{-5}\, V/s$ for both channels when continuously active.
As a significant rise in temperature in the power supply was observed during longer acquisition times, the same experimental setup was repeated with the mainboard and power supply unit being cooled by a fan. The prevention of PCB heating and thus a significantly smaller temperature increase in the analog-to-digital converter was expected to improve the above-mentioned drift characteristics. Figure 4.9 shows the result for a 20-minutes acquisition period.
Using the same linear least squares regression method, the approximated function revealed significantly lower drift: With a resulting negative drift coefficient of $C_{Dc} = -1 \cdot 10^{-6}\, V/s$ for continuous acquisition of one active channel in speed mode, the system being cooled, the drift effects were reduced by more than one order.